

8S651M-RZ Schematics

Revision 1.1

Dte:93/02/19

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	962 (SOUTH BIRDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE,USB
22	Winbond W83697HF
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK,GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL,STR LED,FANS ,CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connecttion
34	TEST POINT

COMPONENT SIDE
(1 oz. Copper)
GND SIDE
(1 oz. Copper)
VCC SIDE
(1 oz. Copper)
SOLDER SIDE
(1 oz. Copper)

GIGABYTE

TitleCOVER SHEET

SizeCustom

Document Number8S651M-RZ

Rev1.1

Date星期一 六月 07, 2004

Sheet1 of 32

Model Name: 8S651M-RZ

Version: 1.1

Component value change history

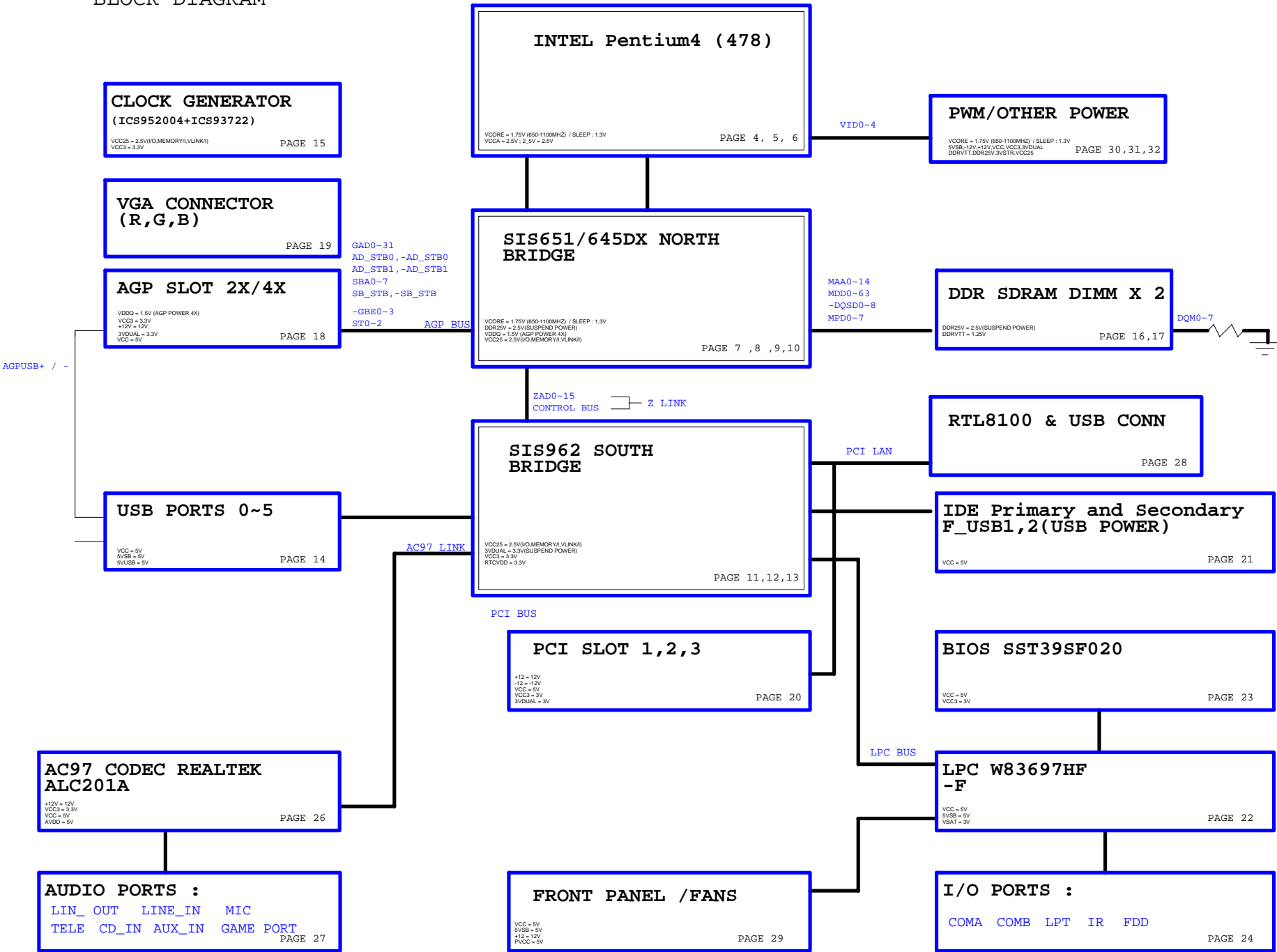
AUTOBOM
2003/09/08

[illegible]

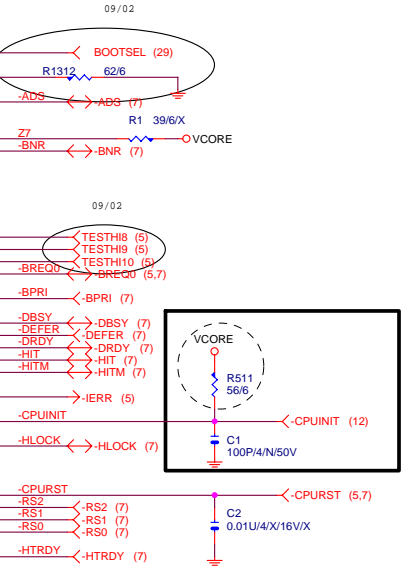
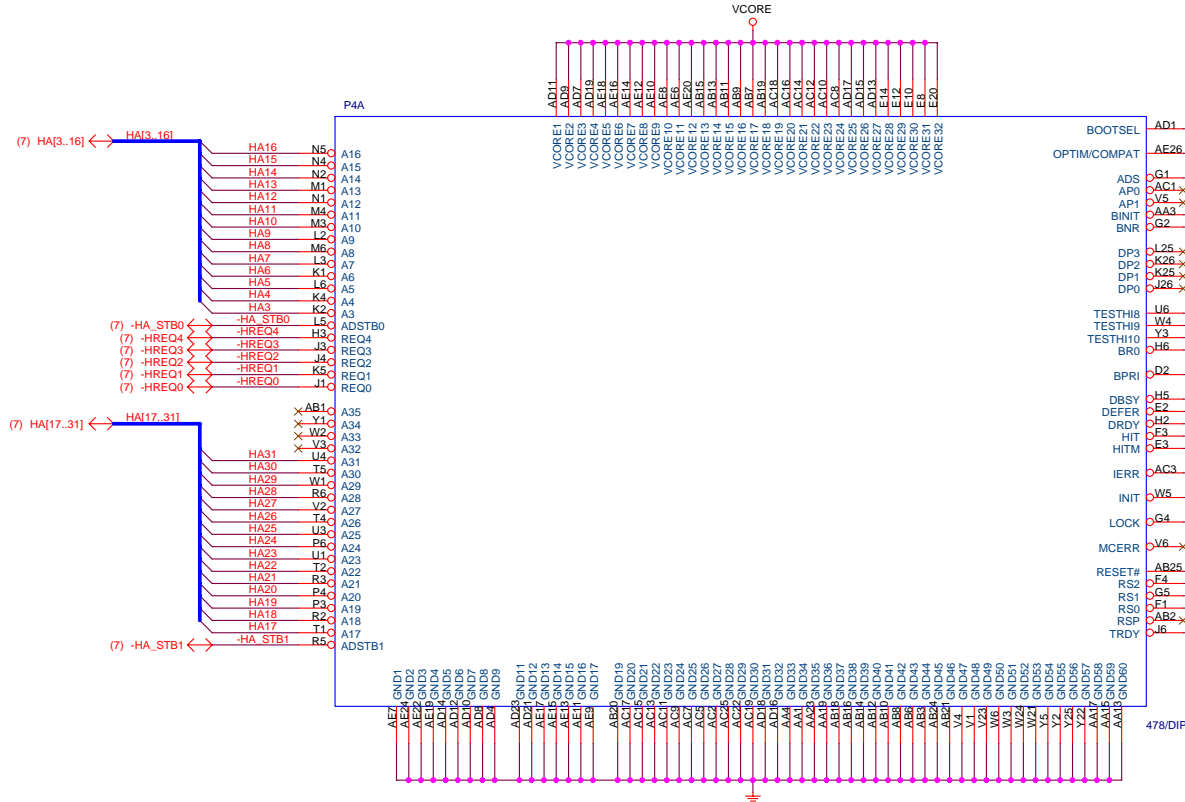
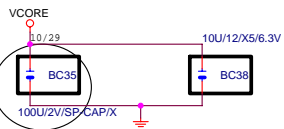
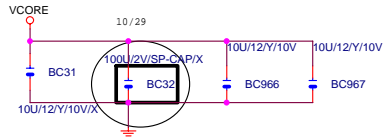
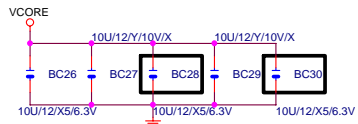
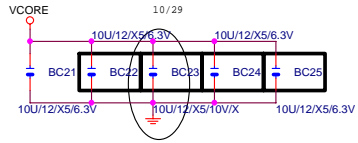
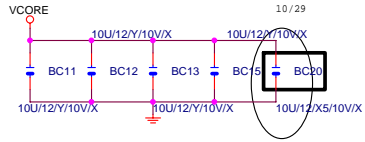
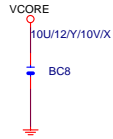
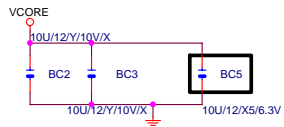
Circuit or PCB layout change
for next version

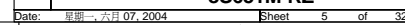
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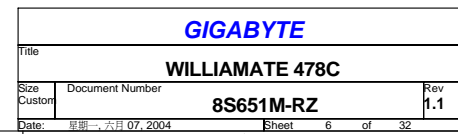
BLOCK DIAGRAM



(X5R) X11 1206(10U) NOTE:GIGA







-DBI[0..3] (6)
-HD[0..63] (6)
-HA[3..31] (4)
-GD[0..31] (18)
-SBA[0..7] (18)
-ST[0..2] (18)

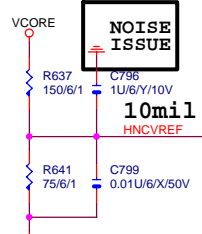
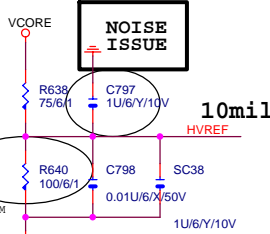
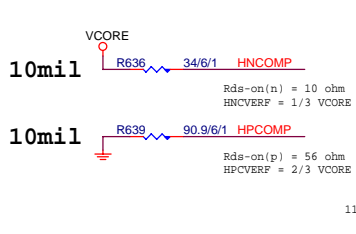
AGP
651/645DX-1
HOST

(15) HCLK HCLK AH26
(15) -HCLK -HCLK AH26
(4) -HLOCK -HLOCK U24
(4) -DEFER -DEFER U26
(4) -HTRDY -HTRDY V26
(4,5) CPURST# CPURST# C20
(5) CPUPWOK# NB CPUPWOK# D19
(4) -BPR# -BPR# T27
(4,5) -BREQ0 -BREQ0 U25
(4) -RS2 -RS2 T24
(4) -RS1 -RS1 T26
(4) -RS0 -RS0 U29
(4) -ADS -ADS V28
(4) -HITM -HITM T28
(4) -HIT -HIT U28
(4) -DRDY -DRDY W26
(4) -DBSY -DBSY V24
(4) -BNR -BNR V27
(4) -HREQ4 -HREQ4 W28
(4) -HREQ3 -HREQ3 W29
(4) -HREQ2 -HREQ2 W24
(4) -HREQ1 -HREQ1 W25
(4) -HREQ0 -HREQ0 Y27
(4) -HA_STB1 -HA_STB1 AD24
(4) -HA_STB0 -HA_STB0 AA24

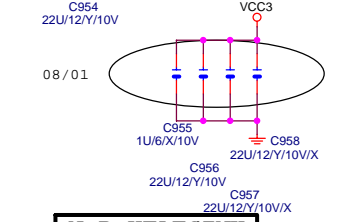
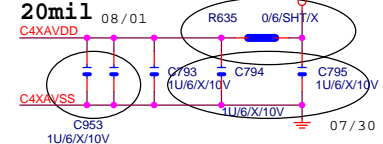
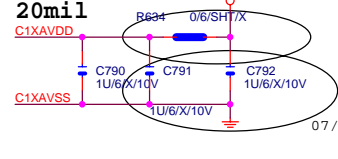
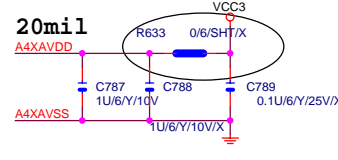
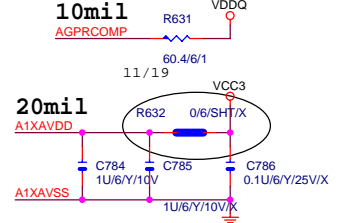
HA31 AE26
HA30 AE25
HA29 AH28
HA28 AD26
HA27 AG29
HA26 AE26
HA25 AE26
HA24 AC24
HA23 AG28
HA22 AD28
HA21 AD28
HA20 AC25
HA19 AD27
HA18 AE28
HA17 AE27
HA16 AB24
HA15 AB26
HA14 AC28
HA13 AC26
HA12 AC29
HA11 AA26
HA10 AB28
HA9 AB27
HA8 AA25
HA7 AA29
HA6 AA28
HA5 Y26
HA4 Y24
HA3 Y28

HOST

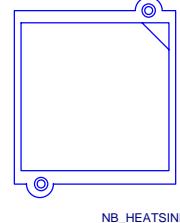
HD#63
HD#62
HD#61
HD#60
HD#59
HD#58
HD#57
HD#56
HD#55
HD#54
HD#53
HD#52
HD#51
HD#50
HD#49
HD#48
HD#47
HD#46
HD#45
HD#44
HD#43
HD#42
HD#41
HD#40
HD#39
HD#38
HD#37
HD#36
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HD#24
HD#23
HD#22
HD#21
HD#20
HD#19
HD#18
HD#17
HD#16
HD#15
HD#14
HD#13
HD#12
HD#11
HD#10
HD#9
HD#8
HD#7
HD#6
HD#5
HD#4
HD#3
HD#2
HD#1
HD#0
DB#3
DB#2
DB#1
DB#0



place this capacitor under 650 solder side VREF C-CAP PULL-UP MEASURE NOISE WORST.



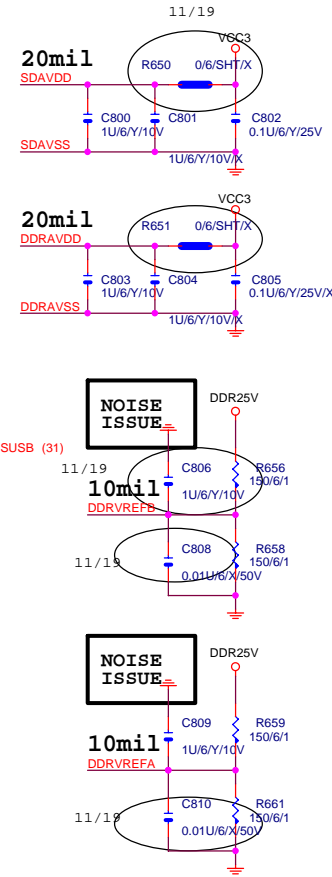
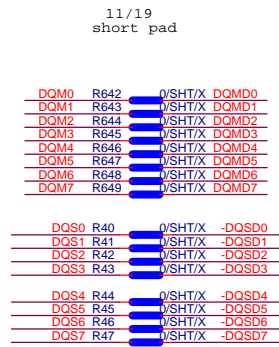
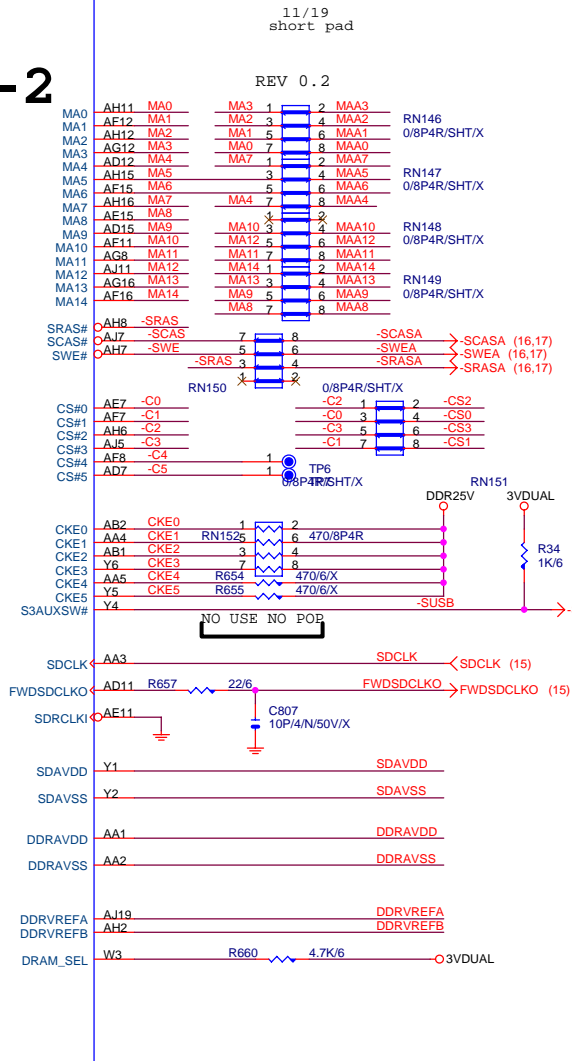
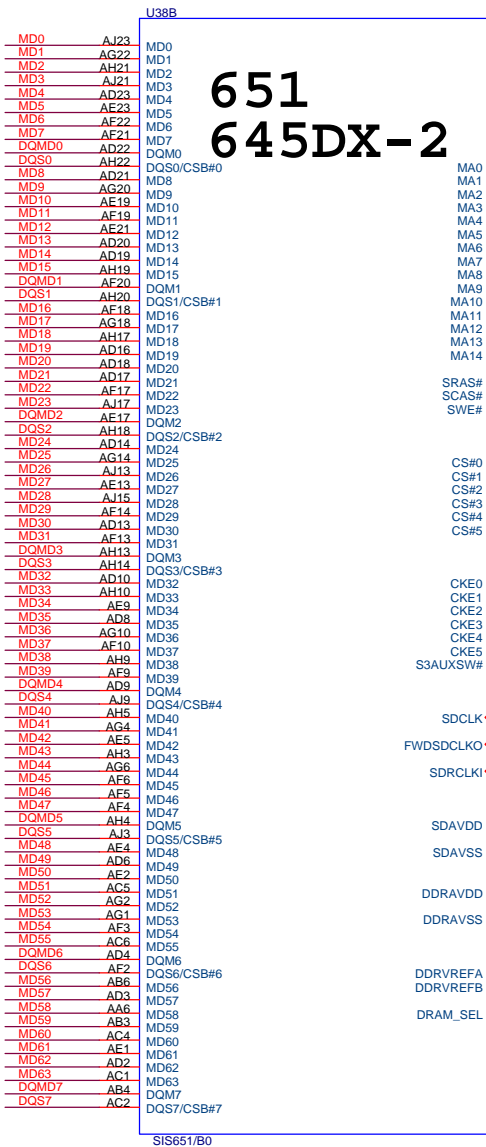
N.B HEATSINK



NB_HEATSINK1

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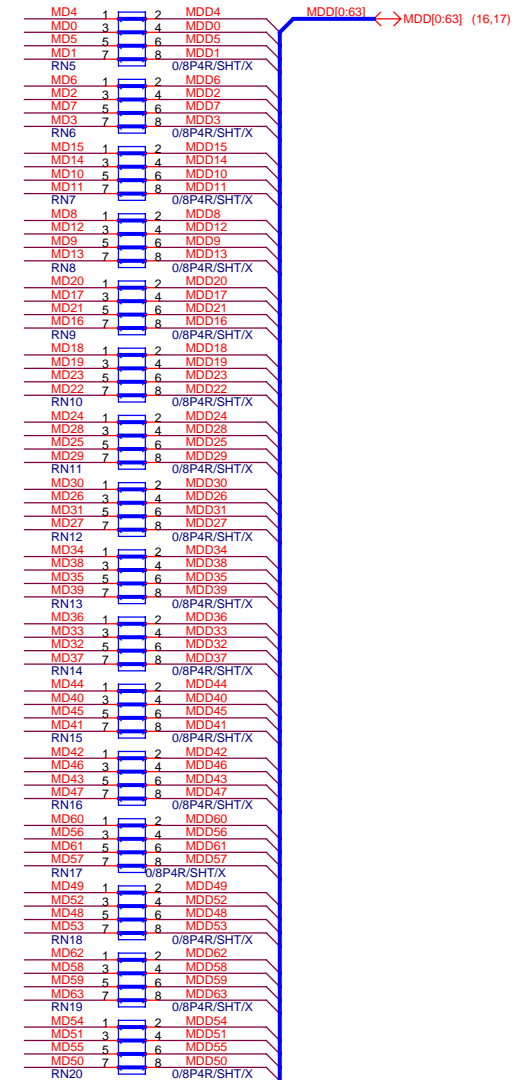
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SIS651/645DX(HOST/AGP)		
Size	Document Number	Rev
Custom	8S651M-RZ	1.1
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DDR MD DAMPPING

Near DIMM 1

11/19 short pad

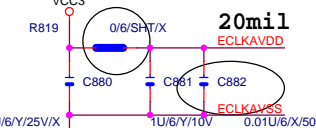
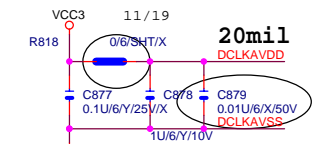
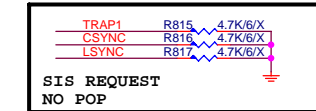
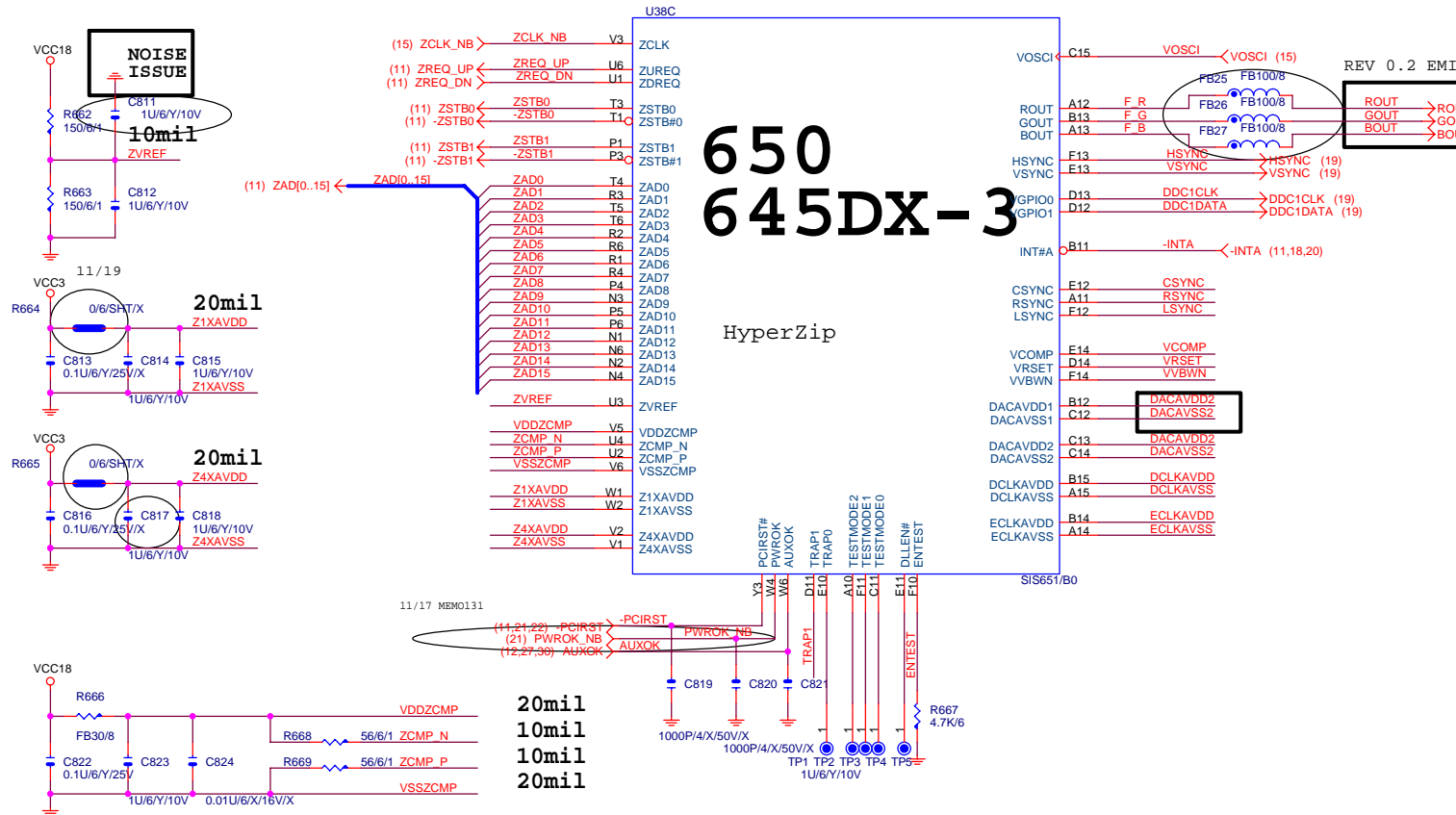


GIGABYTE

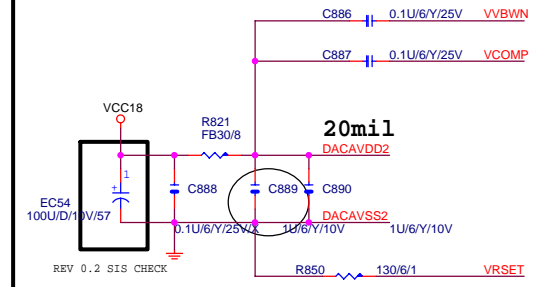
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Size	Document Number	8S651M-RZ			Rev
Custom					1.1
Date:	星期一, 六月 07, 2004	Sheet	8	of	32

VREF C-CAP PULL-UP MEASURE NOISE WORST.

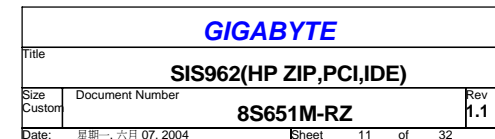
	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SCR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)			0
CSYNC	enable VB			0
RSYNC	enable VGA interrupt			1
LSYNC	enable panel link			0

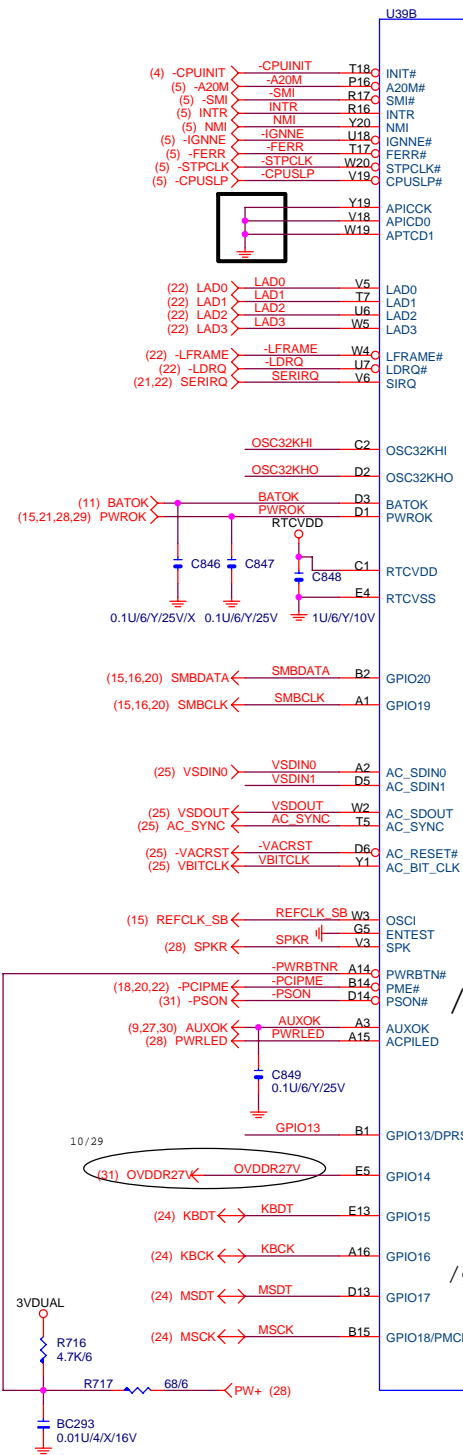


DACAVDD1(VSS)---->DACAVDD2(VSS)
(SIS AP-02)

**GIGABYTE**

Title			
SIS651/645DX(HYPER ZIP)			
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CPU_S

APIC

LPC

RTC

GPIO

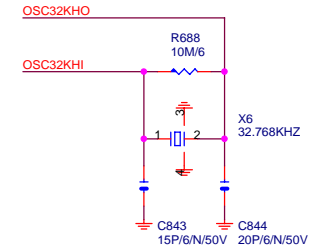
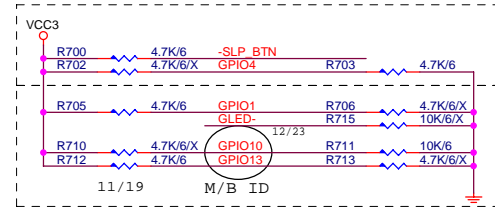
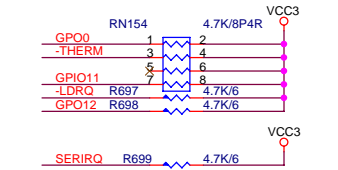
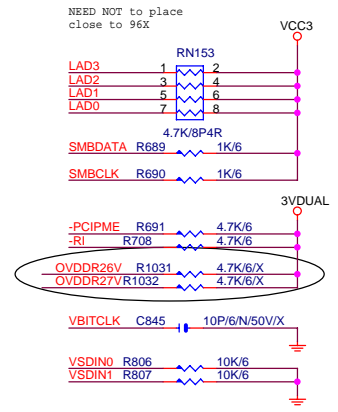
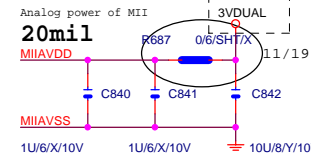
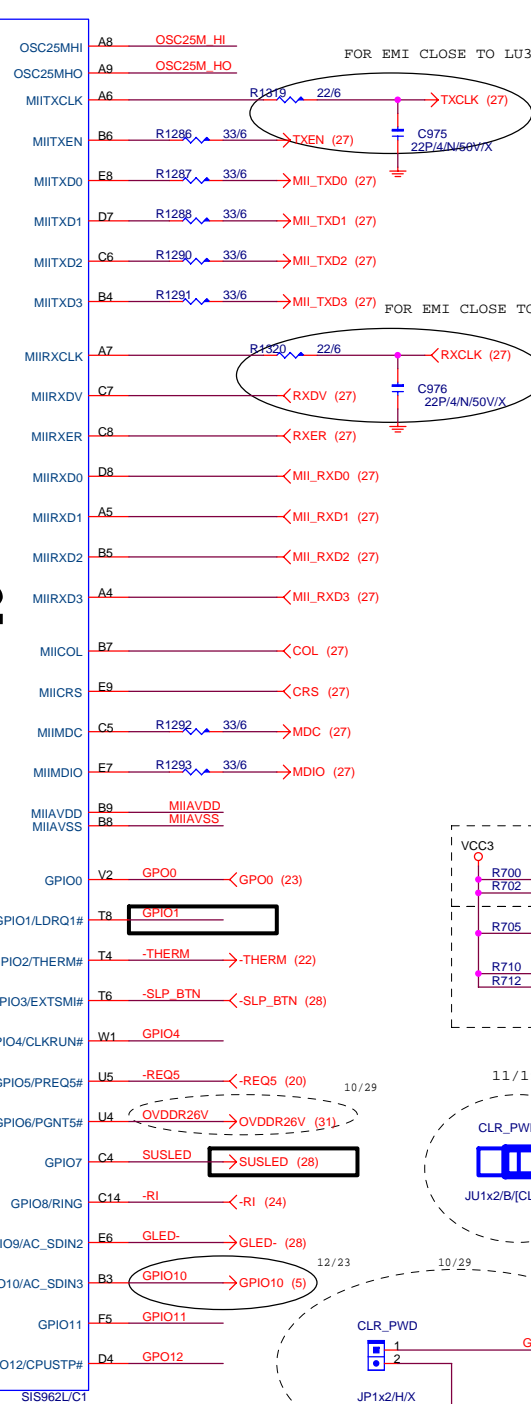
AC97

ACPI
/others

KBC
/geyserville

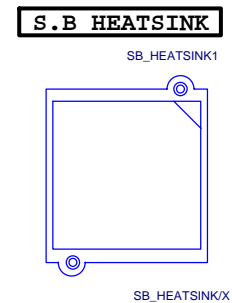
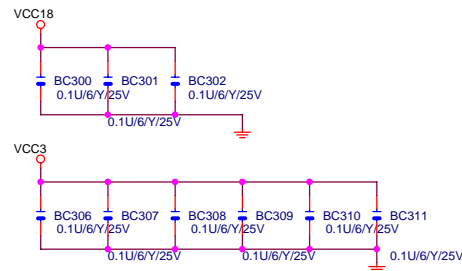
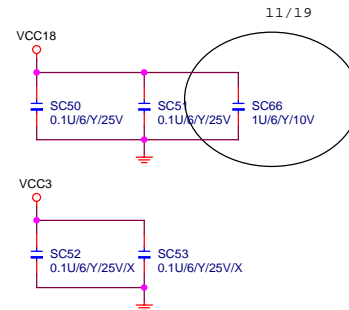
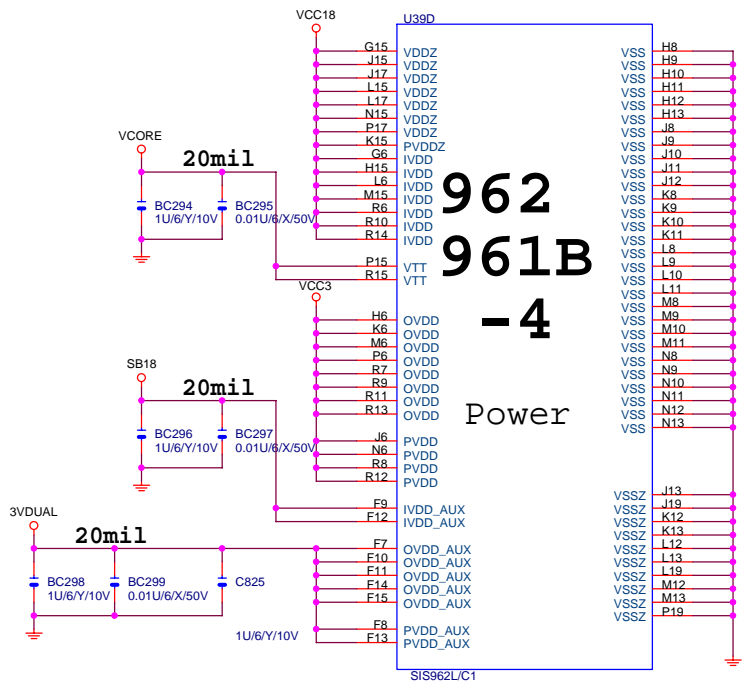
MII

GPIO

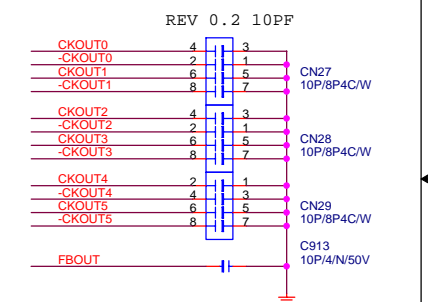
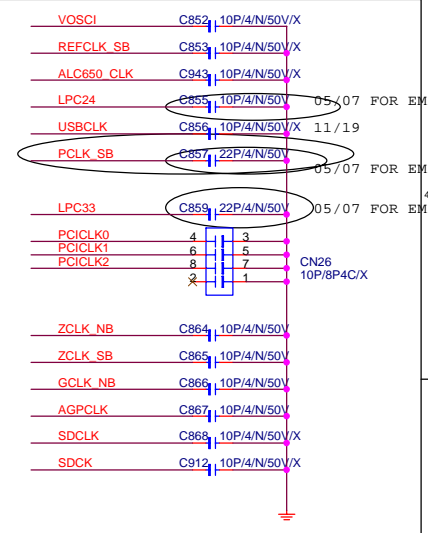
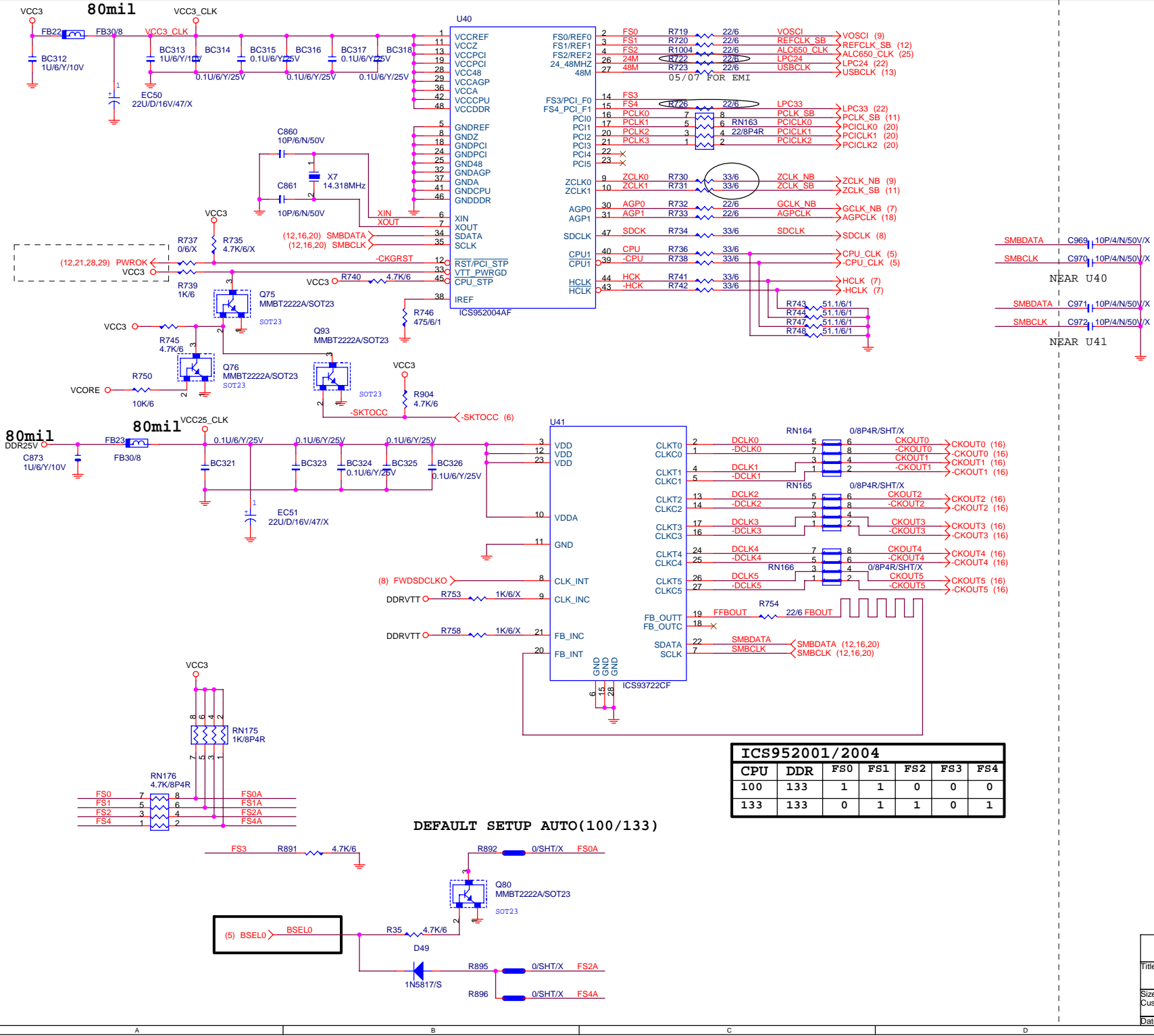


INPUT	REV: 2.0 / 2.1	REV: 3.0	
GPIO1	HI	HI	
GPIO4	LOW	LOW	
GPIO13	LOW	HI	

GIGABYTE			
Title			
SIS962/961B(CPU,LPC,RTC,AC97,GPIO,ACPI,KBC)			
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GIGABYTE			
Title			
SIS962/961B(PWR)			
Size	Document Number	Rev	
Custom	8S651M-RZ	1.1	
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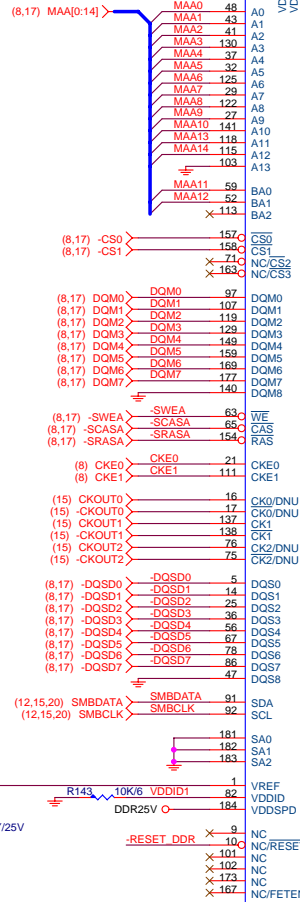
DCLK +/----->0 ohm ADD CAP 10PF (clear glitch)

ICS952001/2004						
CPU	DDR	FS0	FS1	FS2	FS3	FS4
100	133	1	1	0	0	0
133	133	0	1	1	0	1

DEFAULT SETUP AUTO(100/133)

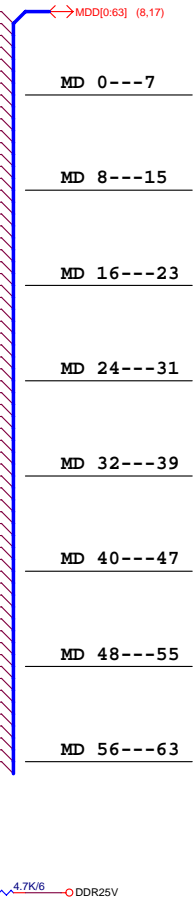
DDR SDRAM 1,2

SIS ONLY MAA

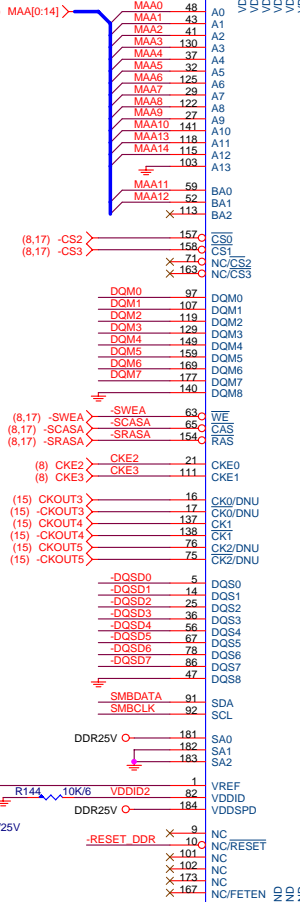


DDR25V

DDR MD GROUP SWAP

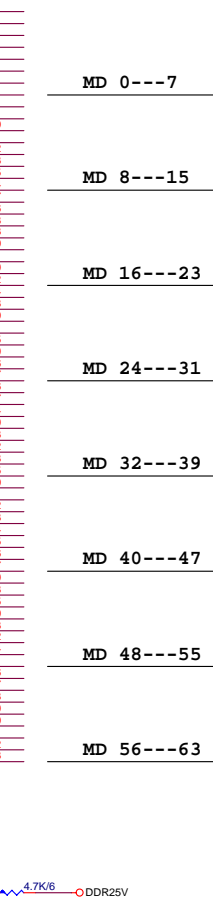


SIS ONLY MAA



DDR25V

DDR MD GROUP SWAP



For Register DDR Support

DDR25V

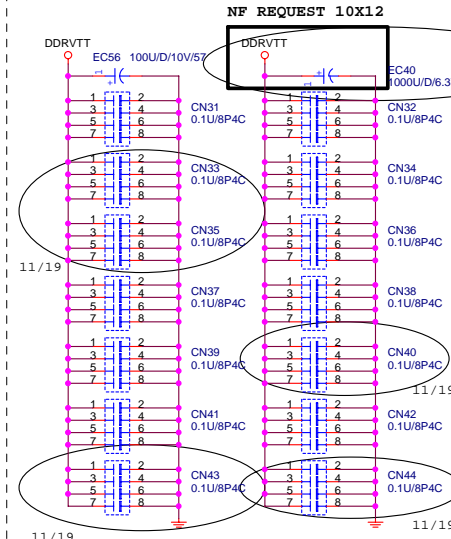


GIGABYTE

DDR UNBUFFERED 1,2

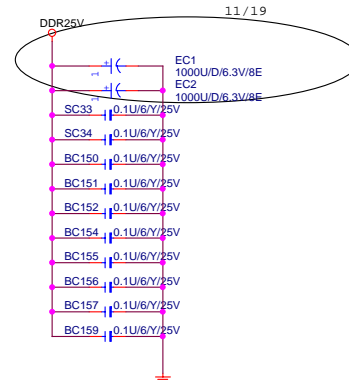
Title	Document Number	Rev
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DDRVTT Decouple



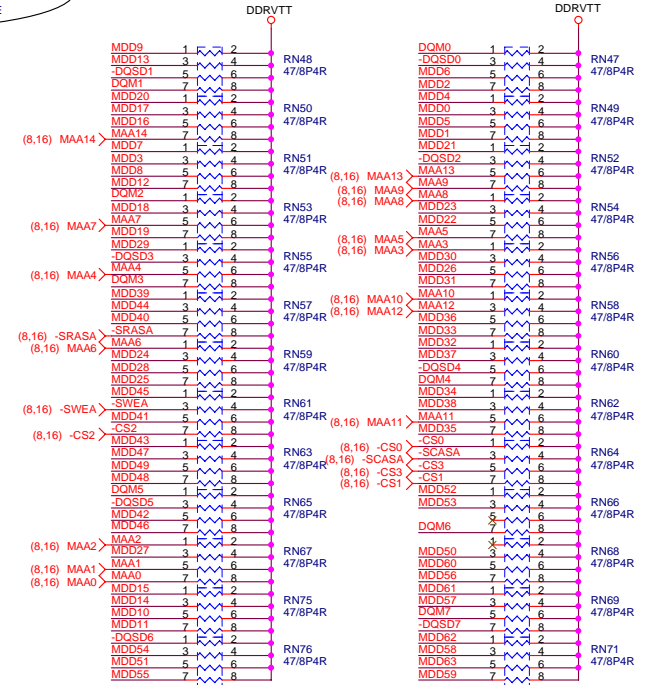
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling capacitor for each two R-packs)

DDR25V Decouple

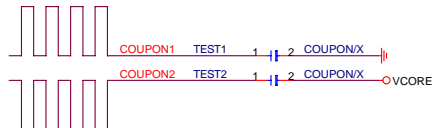


DDR TERMINATION

REV 0.2 DDR DIMM ISSUE
33-->47 OHM



IMPEDENCE TESTING COUPON



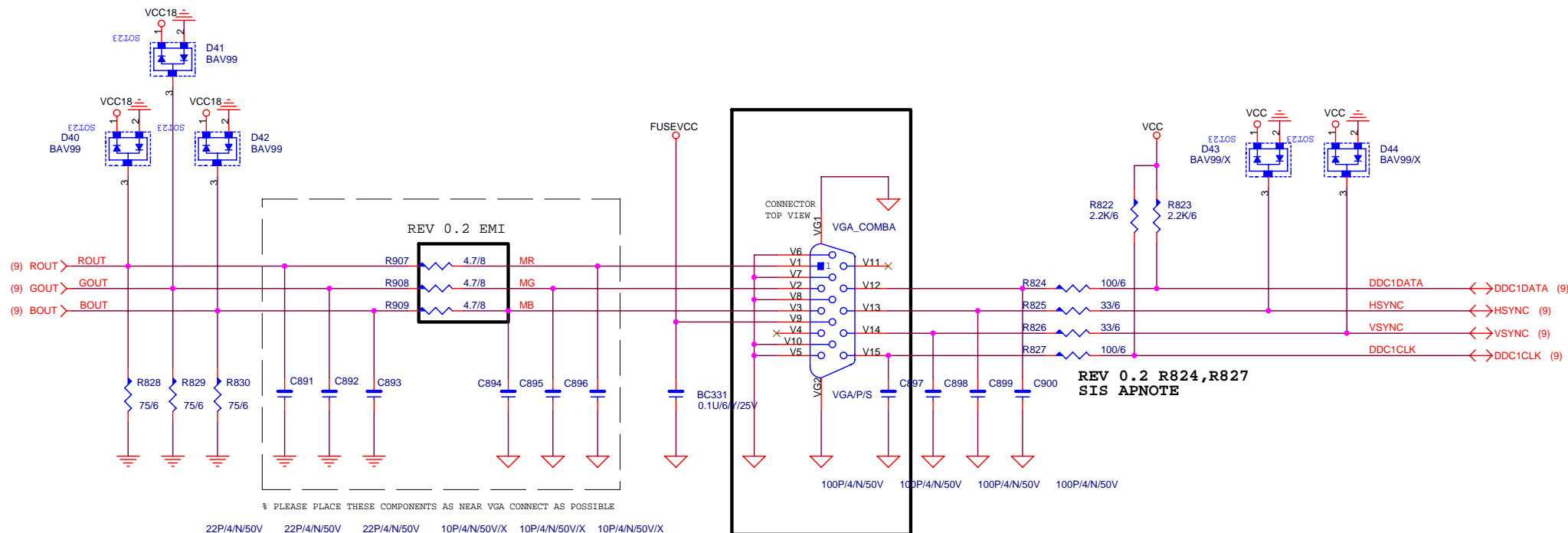
GIGABYTE

DDR UNBUFFERED 3

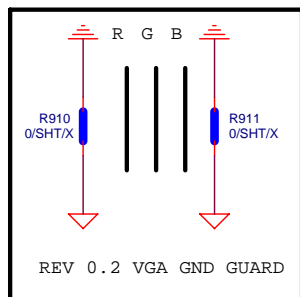
Size	Document Number	Rev
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VGA CONNECTOR 1

SIS 645DX NO POP



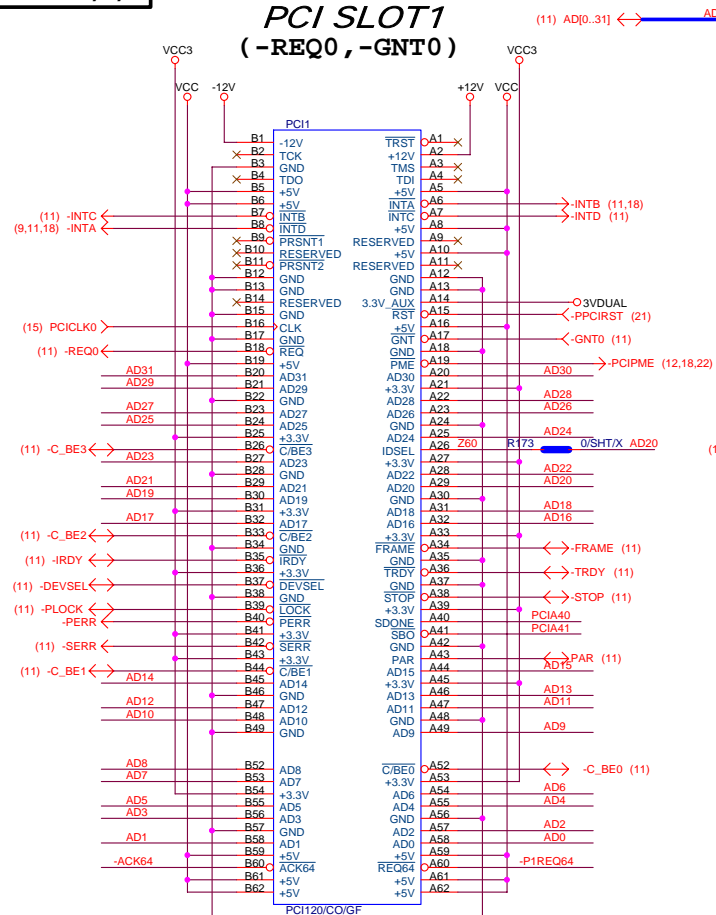
DUAL LAYOUT (VGA/COM)



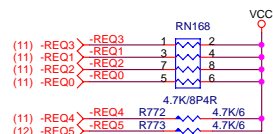
GIGABYTE		
Title		
VGA CONNECTOR		
Size	Document Number	Rev
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PCI SLOT 1,2,3

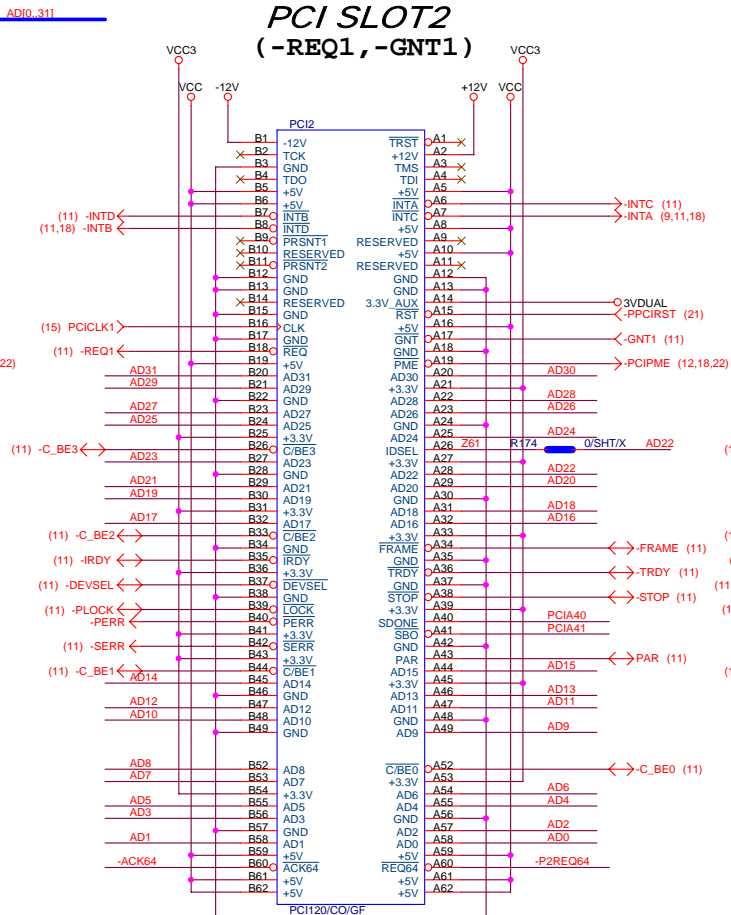
PCI SLOT1
(-REQ0, -GNT0)



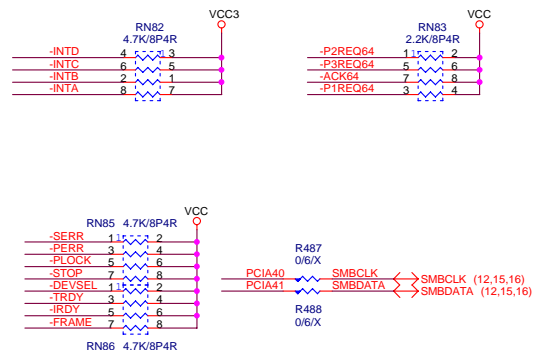
SIS--IDSEL(A20)
(B)



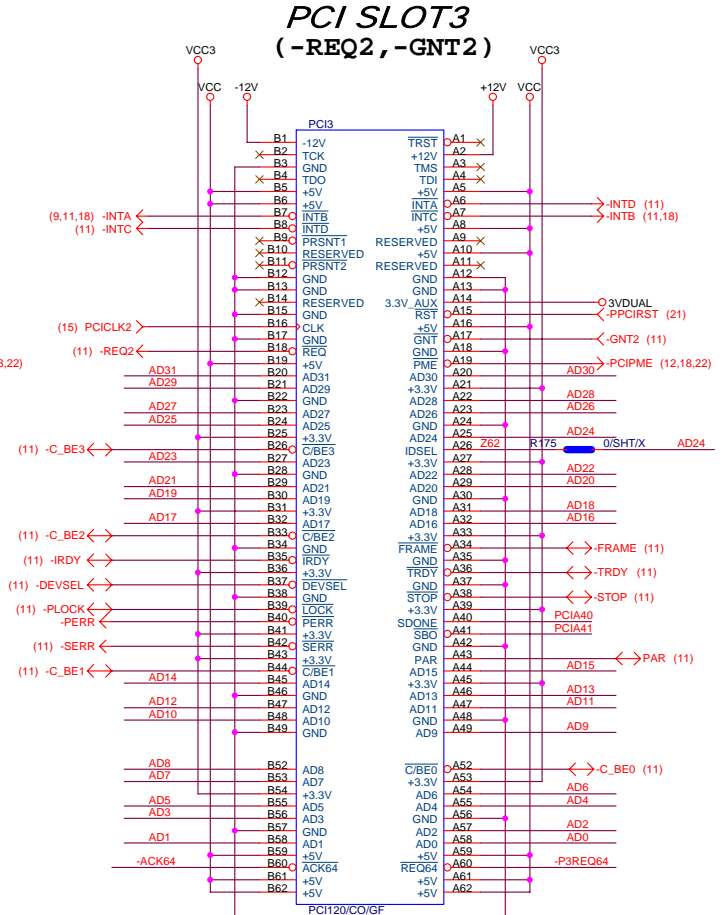
PCI SLOT2
(-REQ1,-GNT1)



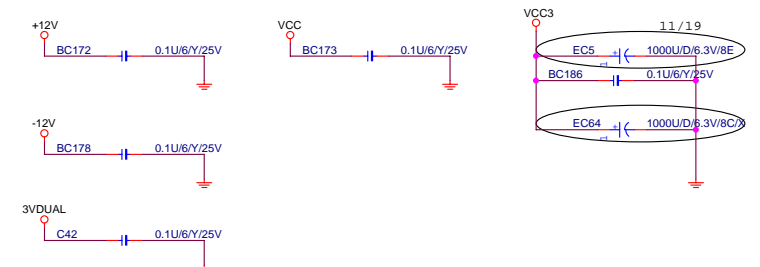
SIS--IDSEL(A22)
(C)



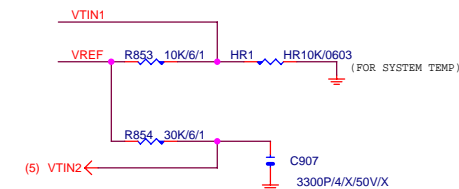
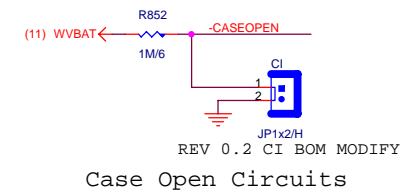
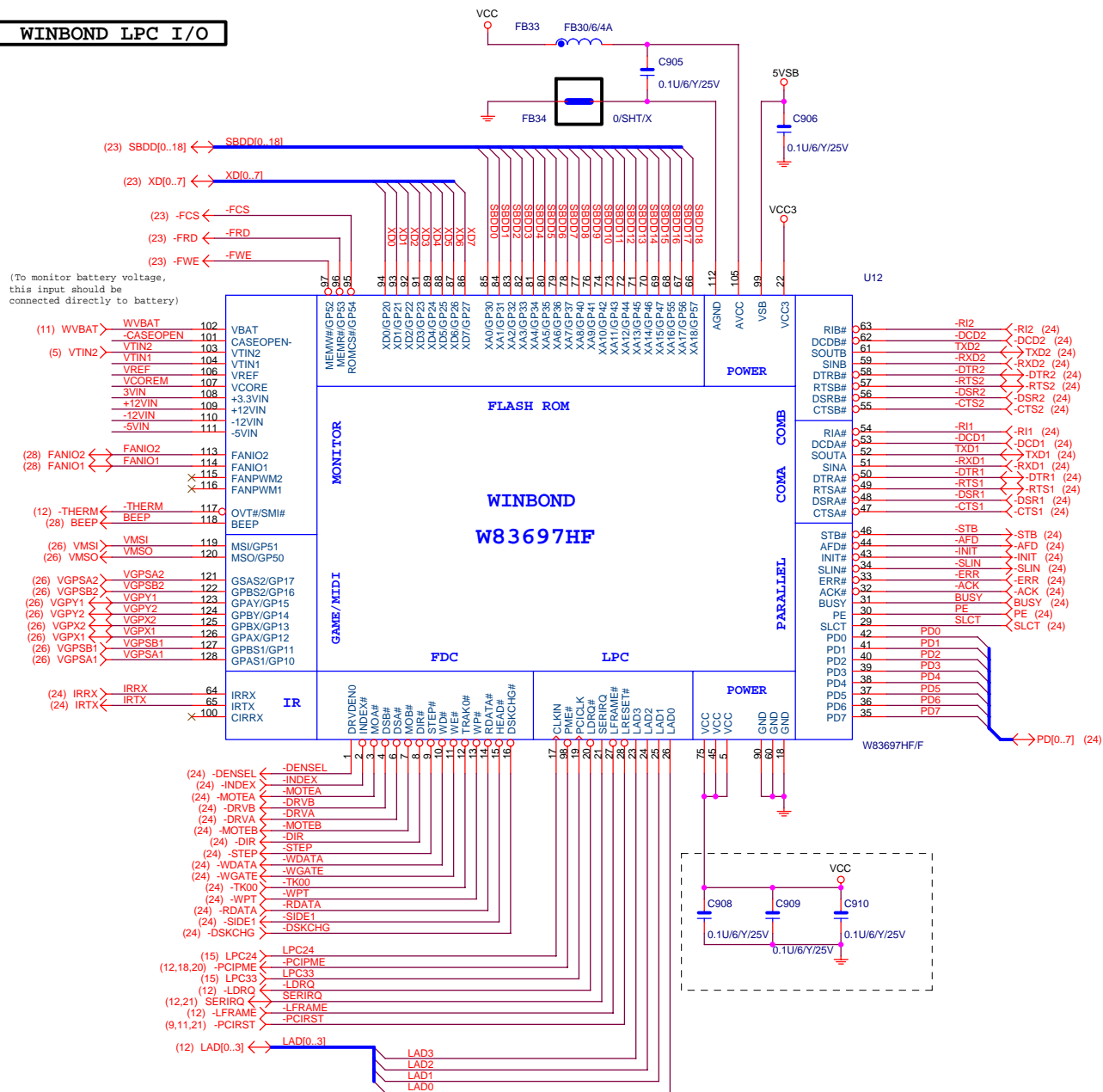
PCI SLOT3
(-REQ2,-GNT2)



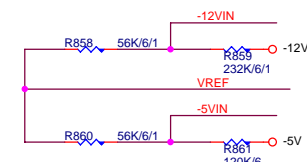
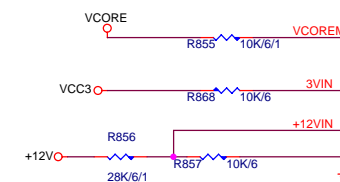
SIS--IDSEL(A24)
(D)



WINBOND LPC I/O



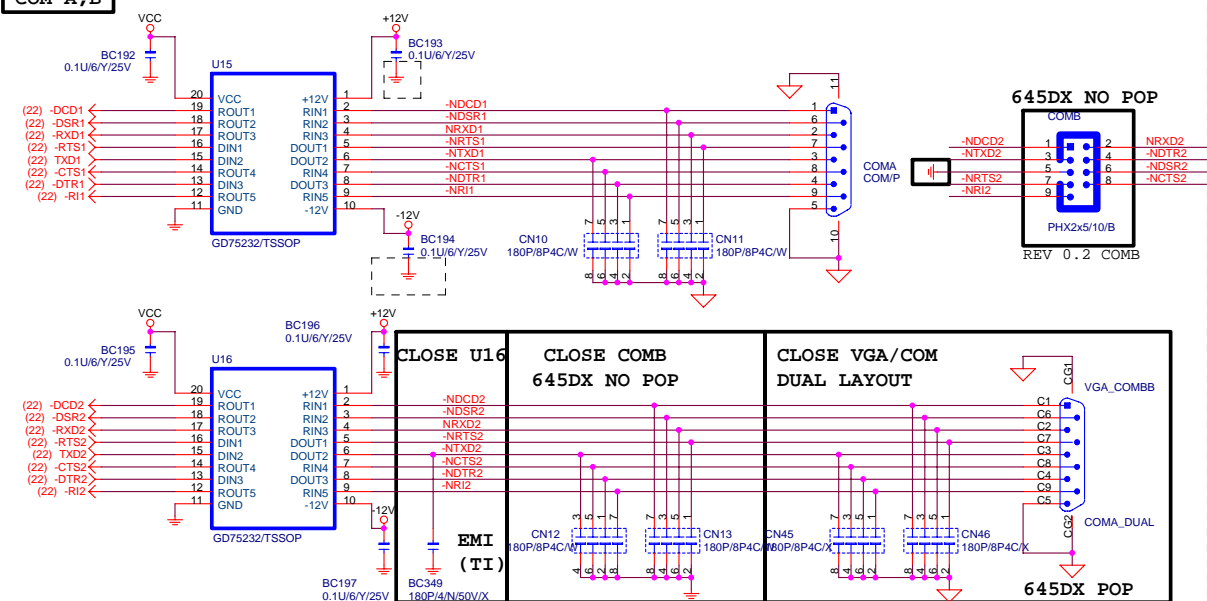
Thermal Monitoring



Voltage Monitoring

GIGABYTE				
LPC W83697				
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COM A,B



WAKE UP

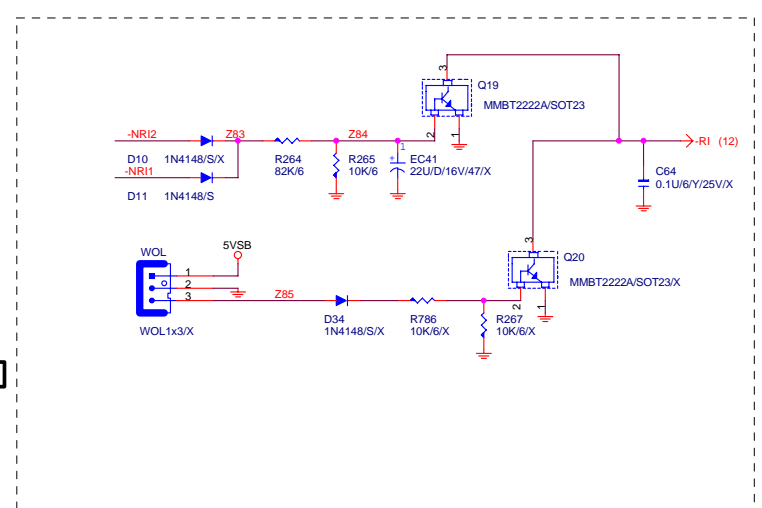
RING IN

WAKE ON LAN

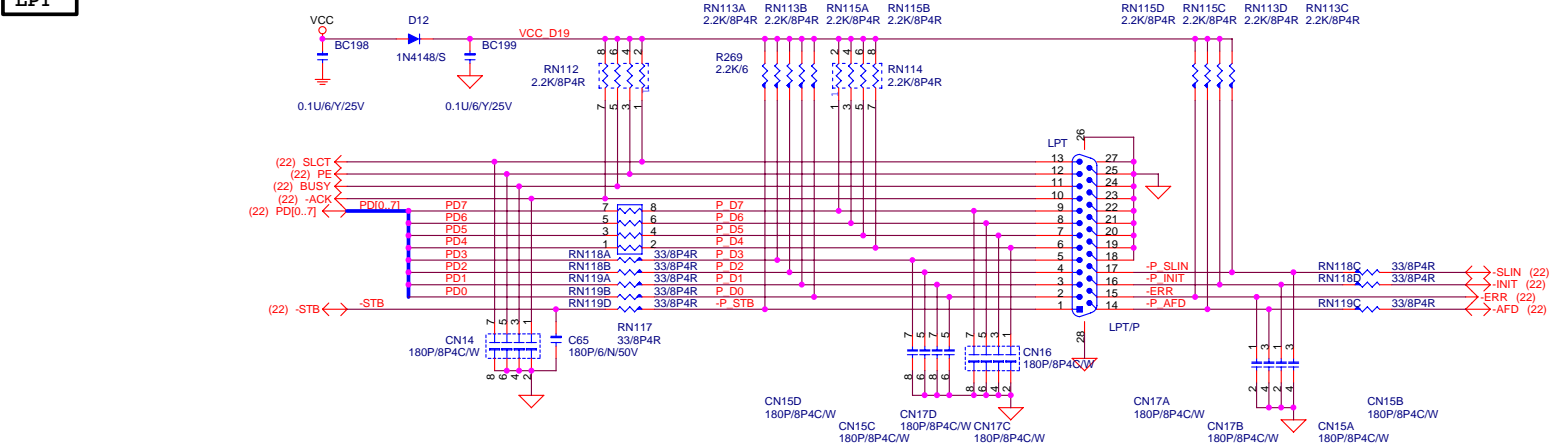
LAN WAKEUP

RING POWER ON

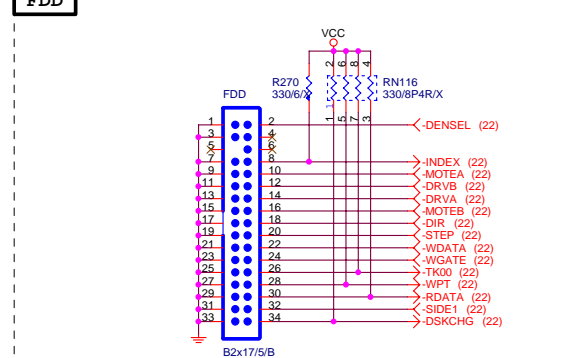
MODEM WAKEUP



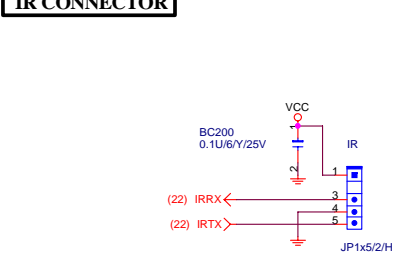
LPT



FDD

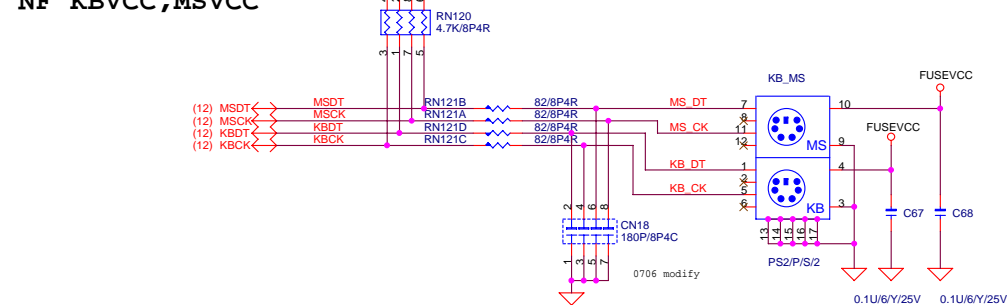


IR CONNECTOR

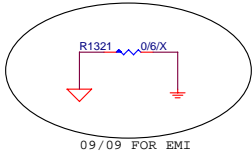


KBC/PS2

NF KBVCC,MSVCC



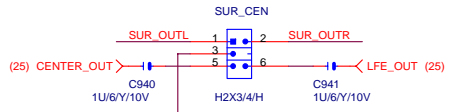
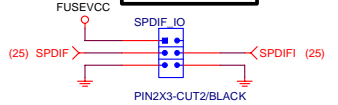
GIGABYTE		
Title		
COM,PRT,FDD,KB,IR		
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Title AUDIO (AC97 CODEC)			
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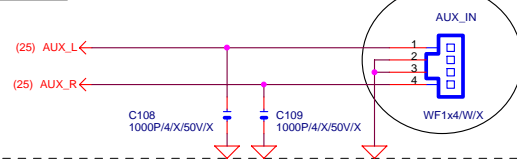
SPDIF

SPDIF_IO



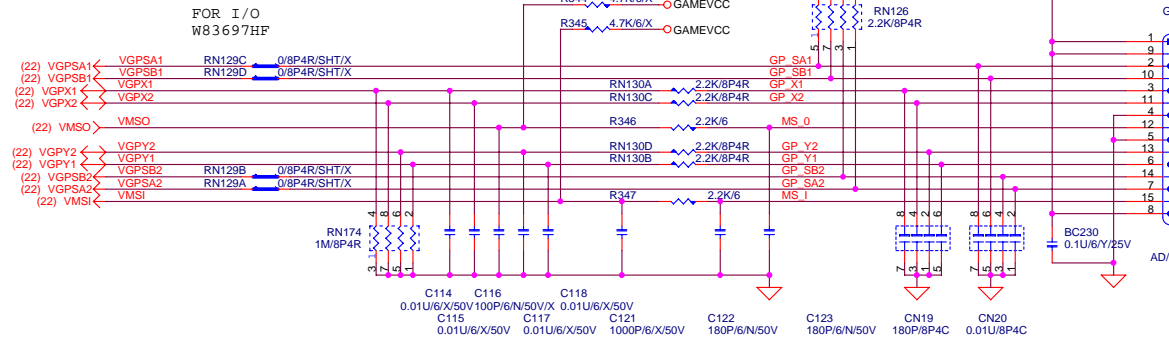
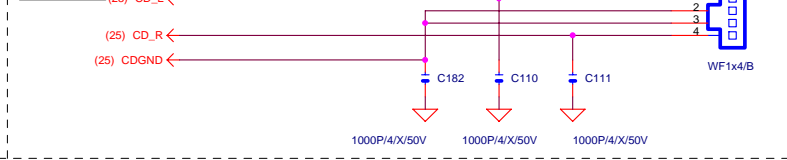
AUX IN

DISTI DEFAULT NO POP

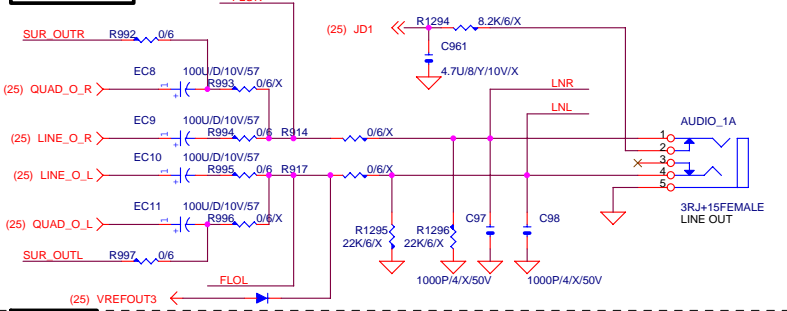


GAME PORT

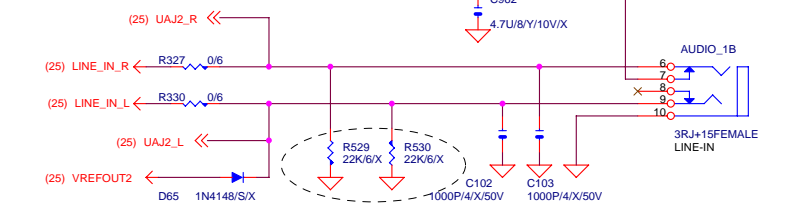
CD IN



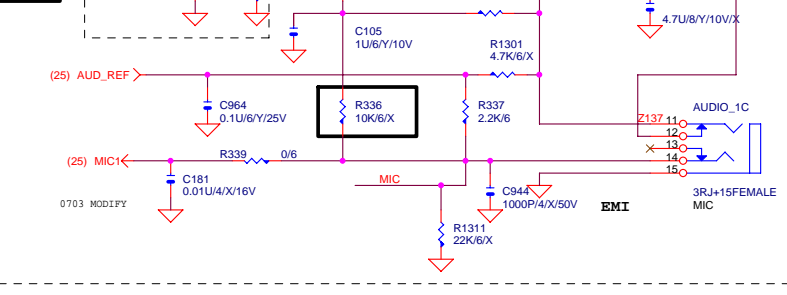
LINE OUT



LINE-IN



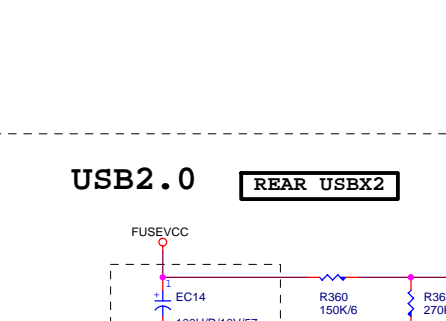
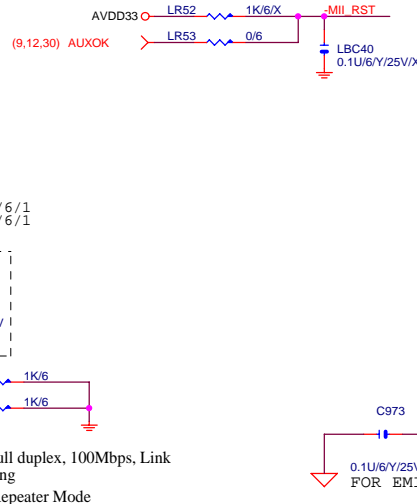
MIC



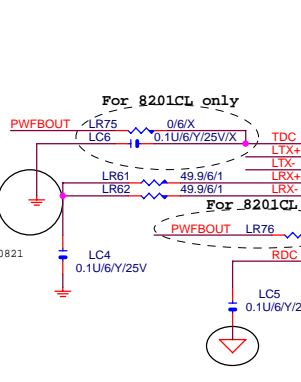
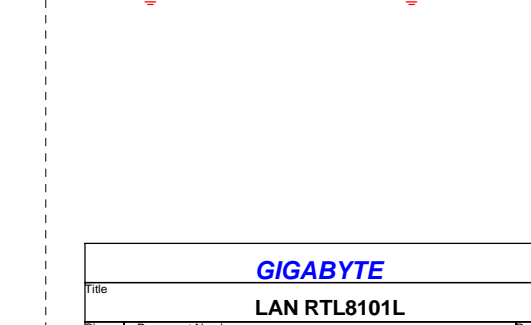
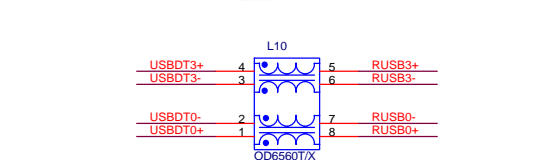
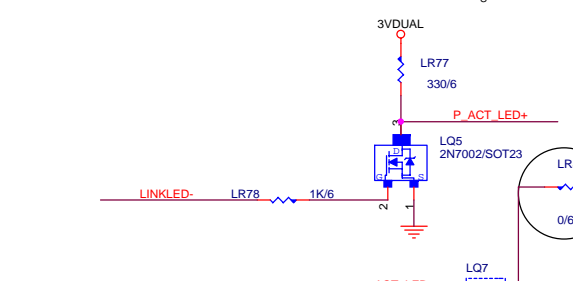
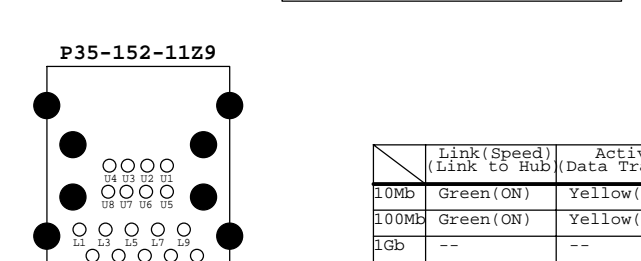
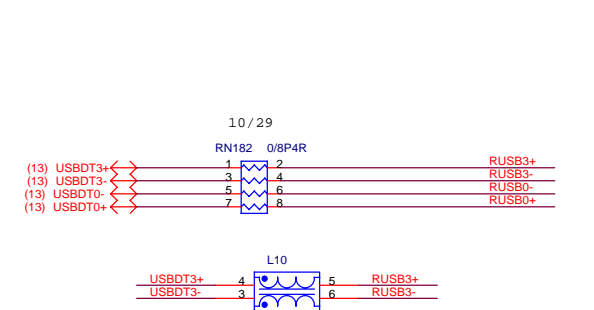
GIGABYTE			
Title			
AUDIO OUTPUT, GAME PORT			
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MII
: 4 6 /


LU3




REAR USBX2




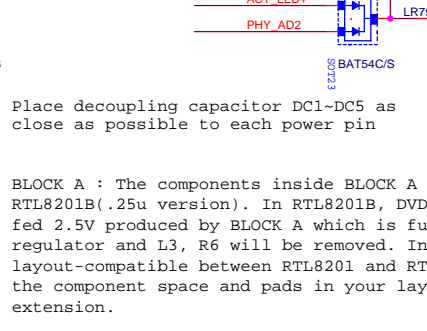
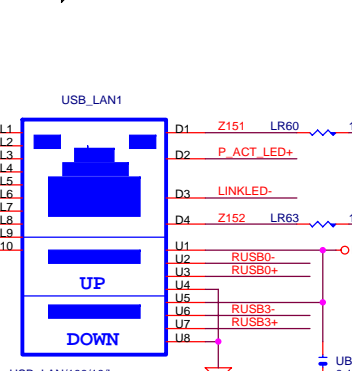
Dual Color LED

D4  D3 Green

D4  D3 Orange

Single Color LED

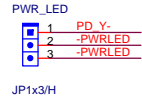
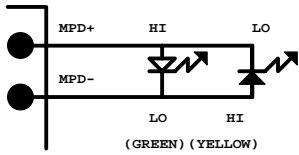
D2  D1 Yellow



BLOCK A : The components inside BLOCK RTL8201B(.25u version). In RTL8201B, fed 2.5V produced by BLOCK A which is regulator and L3, R6 will be removed. layout-compatible between RTL8201 and the component space and pads in your extension.

FRONT PANEL

PWR_LED FOR DISTI PIN 1X3 LED USED



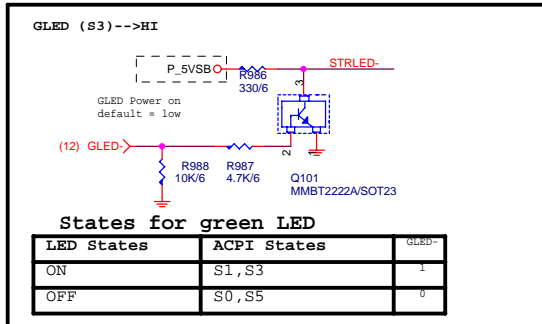
LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

CPU_FAN

W=0.167W

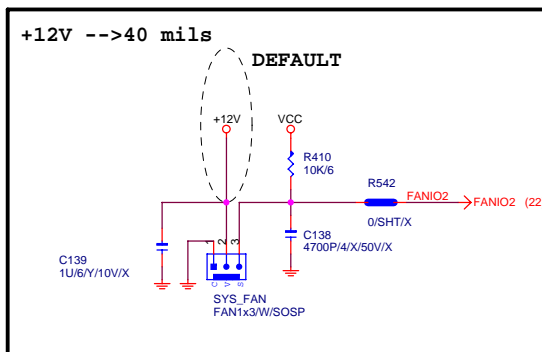


States for green LED

LED States	ACPI States	GLED
ON	S1,S3	1
OFF	S0,S5	0

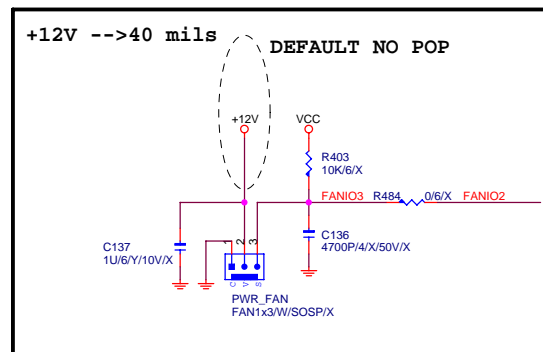
SYSTEM FAN

W=0.167W

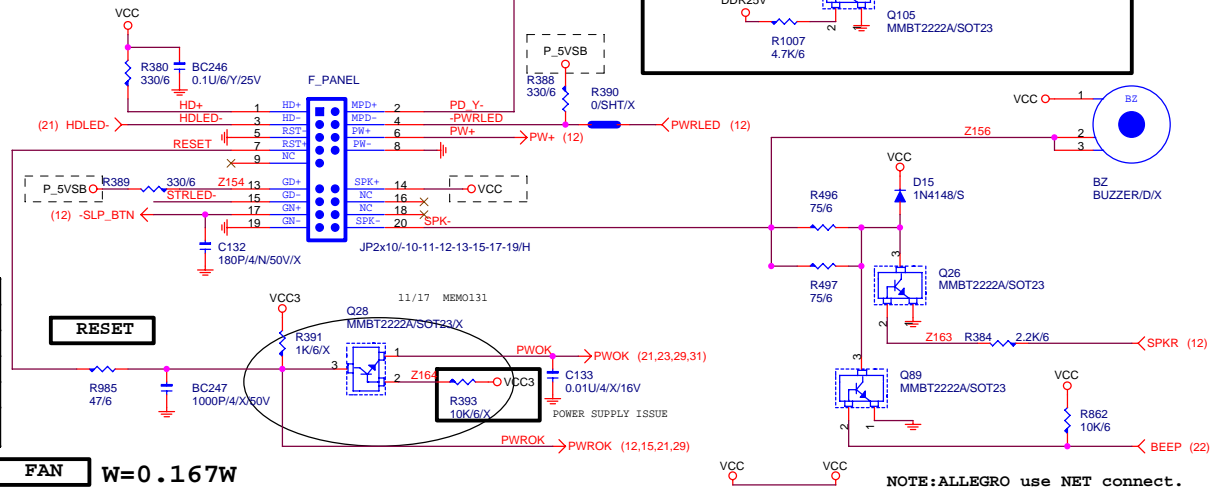
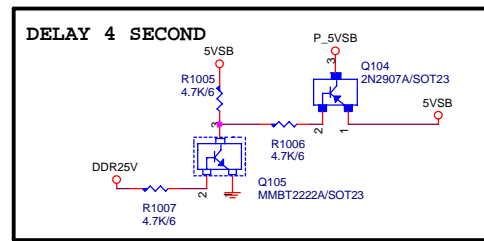


POWER FAN

W=0.167W

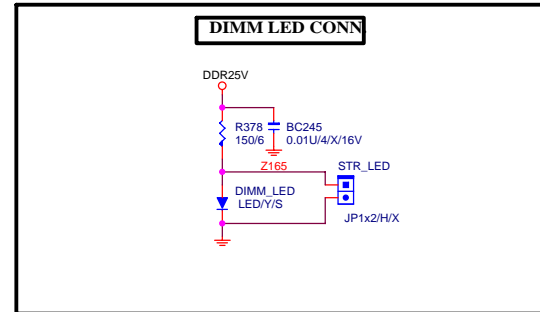


DELAY 4 SECOND



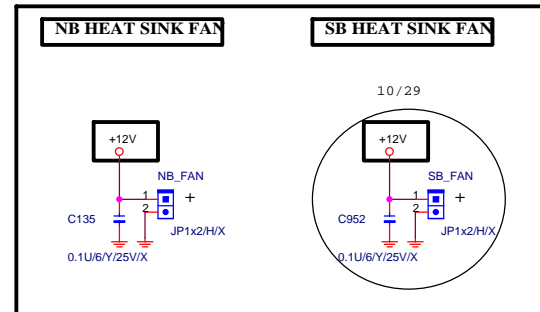
NOTE:ALLEGRO use NET connect.

DIMM LED CONN



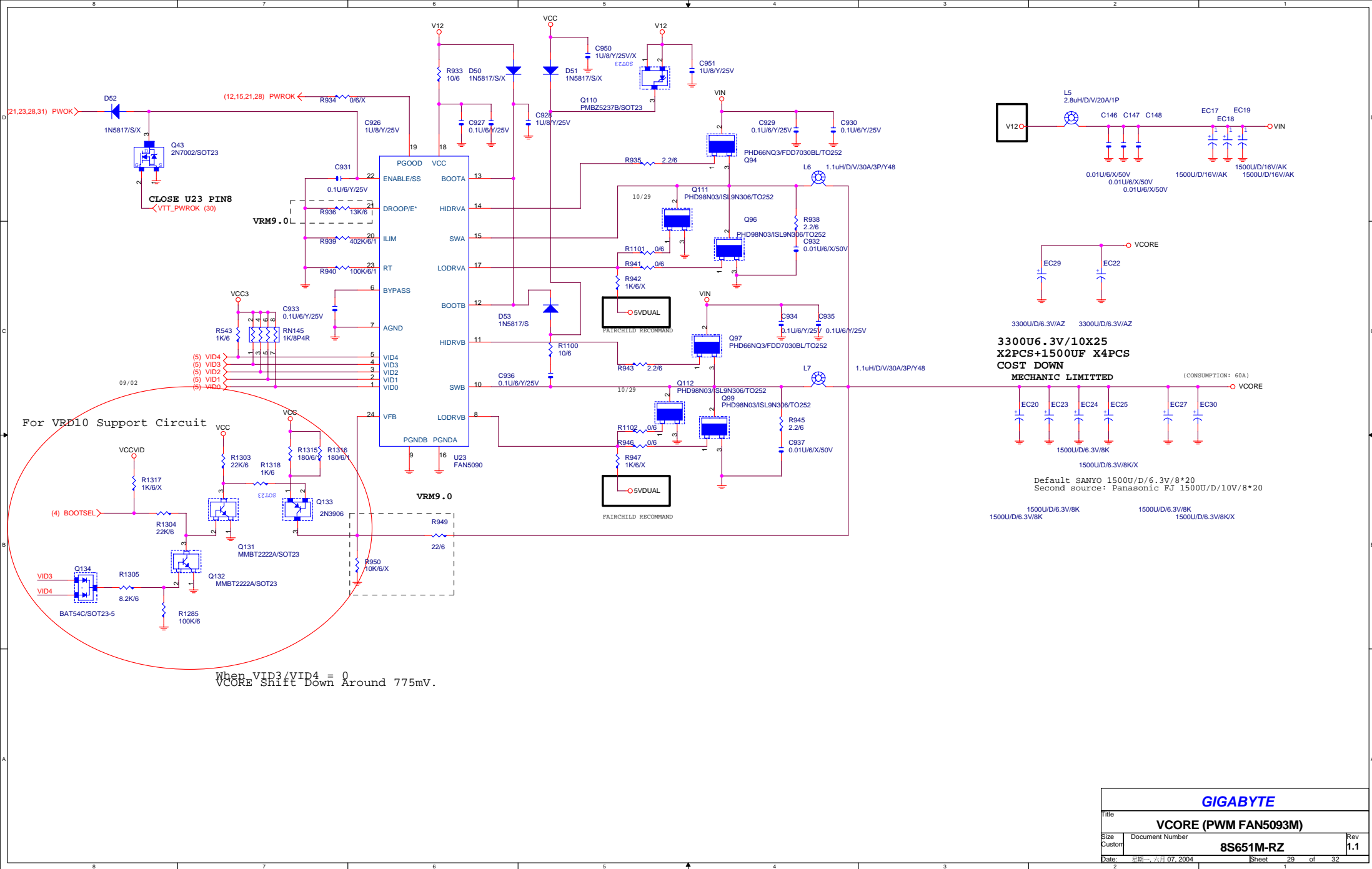
NB HEAT SINK FAN

SB HEAT SINK FAN

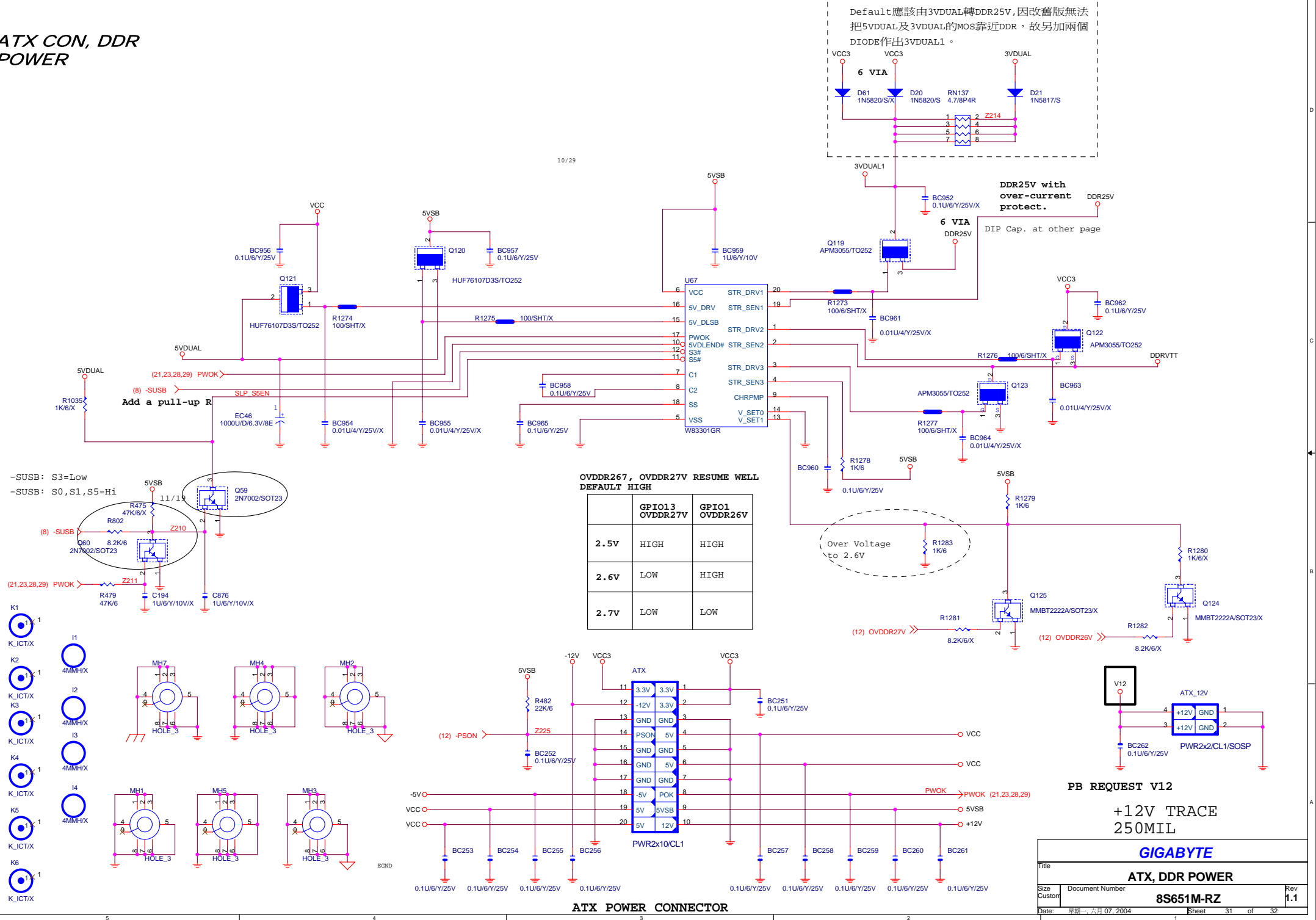


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PANEL, STR LED & FANS		
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*ATX CON, DDR
POWER*



ATX POWER CONNECTOR

PB REQUEST V12

+12V TRACE
250MIL

GIGABYTE

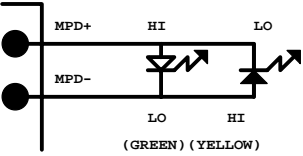
ATX, DDR POWER

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RTL8100L ON-BOARD			
	-REQ0	PCI1	IDSEL(A20)--B
	-REQ1	PCI2	IDSEL(A22)--C
	-REQ2	PCI3	IDSEL(A24)--D
	-REQ3	RTL8100L	IDSEL(A27)--B



States for a single-color power LED

LED States	ACPI States	BIOS			
		MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

States for a dual-color power LED

LED States	ACPI States	BIOS			
		MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	BIOS	
		GPIO9	GPIO9
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO

8SRXL South Bridge GPIO LIST				
ITEM	DESCRIPTION	I/O	STATUS	Default
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi
GPIO1	N/A		PULL-UP	Hi
GPIO2	THERM#			Hi
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi
GPIO4	CLKRUN#		PULL-DOWN	Lo
GPIO5	N/A		PULL-UP	Hi
GPIO6	DDR OVER VOLTAGE	O		Hi
GPIO7	SUSLED	O	AS LIKE DEFINED...	Lo
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi
GPIO9	GLED	I	AS LIKE DEFINED...	Lo
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO11	N/A		PULL-UP	Hi
GPIO12	N/A		PULL-UP	Hi
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO14	DDR OVER VOLTAGE	I		Lo
GPIO15	KB Data	I/OD		
GPIO16	KB Clk	I/OD		
GPIO17	MS Data	I/OD		
GPIO18	MS Clk	I/OD		

BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
			GPIO7	ACPILED	GPIO9		GPIO7	ACPILED	GPIO9		
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

GIGABYTE

Title			
GPIO, REQ/GNT Table			
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